Peripheral Bus Technologies

Small Embedded Systems

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There are a number of bus systems that can be used to connect peripherals to CPUs

of interest are:

- I^2C – Inter Integrated Circuit
- SPI – Serial Peripheral Interface

CAN

Controller Area Network

- Developed as a system for automation in cars
- Networks Electronic Control Units, cars may have upto 80
- Used in industrial automation contexts
- multiple masters multiple slave
- any unit can initiate communications
- bus contention resolved using bitwise arbitration

Max nodes	128
Max bitrate	1000 kbit s^{-1} over 40 m
Max length	1000m at 40kkbit/s

I^2C

Inter Integrated Circuit

- Designed for connecting low speed peripherals
- On PCB or between PCB
- SMBus is a subset
  - Fans, batteries, temperature, lib switches
- multiple master, multiple slave
- bitwise arbitration

Max nodes	127 or 1023
Max bitrate	$3400\,\mathrm{kbit\,s^{-1}}$
Max length	7.6 m

SPI

Serial Peripheral Interface

- Single master, multiple slave
- Full Duplex
  - simultaneous two way comminications
- high speed data
- less PCB than parallel bus
- uses
  - MMC and SD cards
  - JTAG

Part I

Bitwise Arbitration

- CAN and I^2C
  - allow multiple masters
  - have request–responce interaction with slave devices
  - ACK messages
- problem of bus contention
  - two deices transmit simultaneously
- Need for high performance with low overhead
- Carrier sense multiple access / bitwise arbitration (CSMA/BA) scheme used

Carrier sense bitwise arbitration

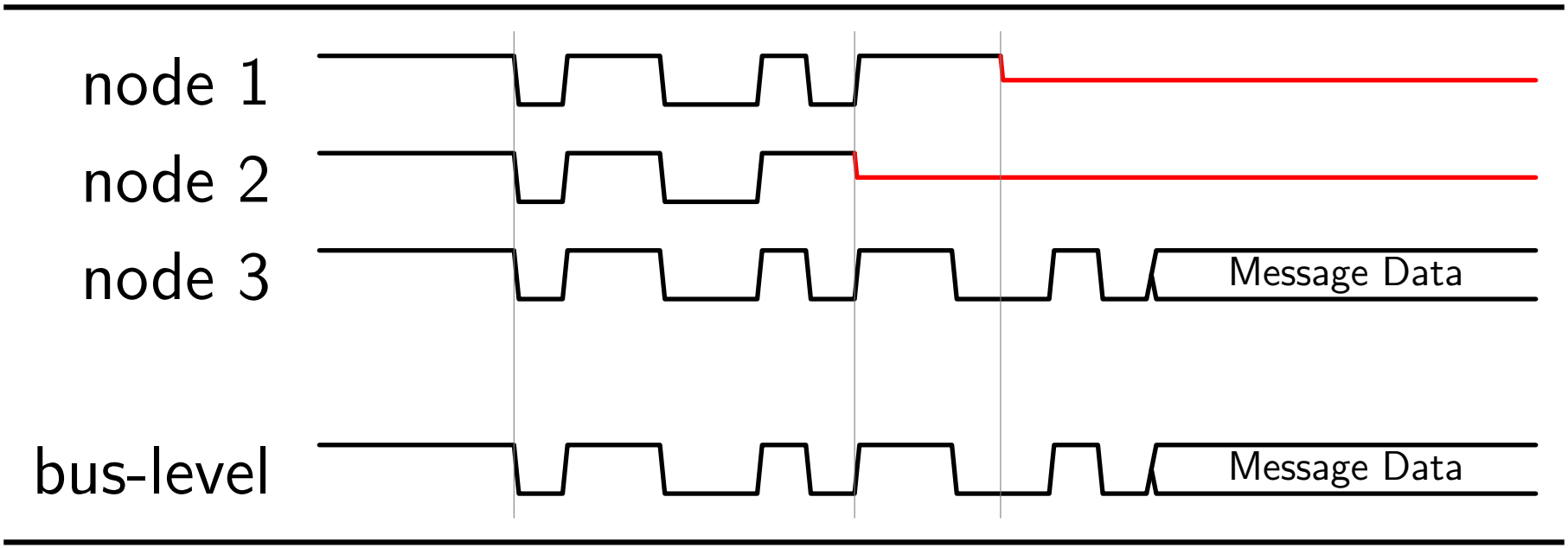
- Buses use serial communications
- Exploit electrical characteristics of bus and driving electronics

Bus behaviour

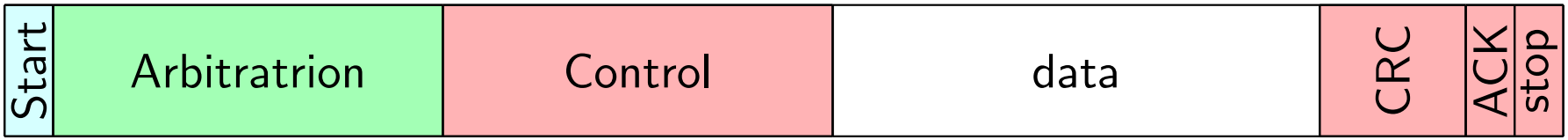
- logical and of signals
  - 0 dominant bit
  - 1 recessive bit
- monitor bus:
  - if writing a 1 and reading 0
  - bus lost to other device

- first field is address
- acts as defacto priority
- low addresses have high priority

Mechanism



1. Nodes write identical header
2. Node 2 drops out first
3. Node 1 drops out second
4. Node 3 continues uninterrupted


Start
Arbitratrion
Control
data
CRC
ACK
stop

John Catsoulis

Designing Embedded Hardware

O'Reilly

Part II

I^2C
Inter Integrated Circuit

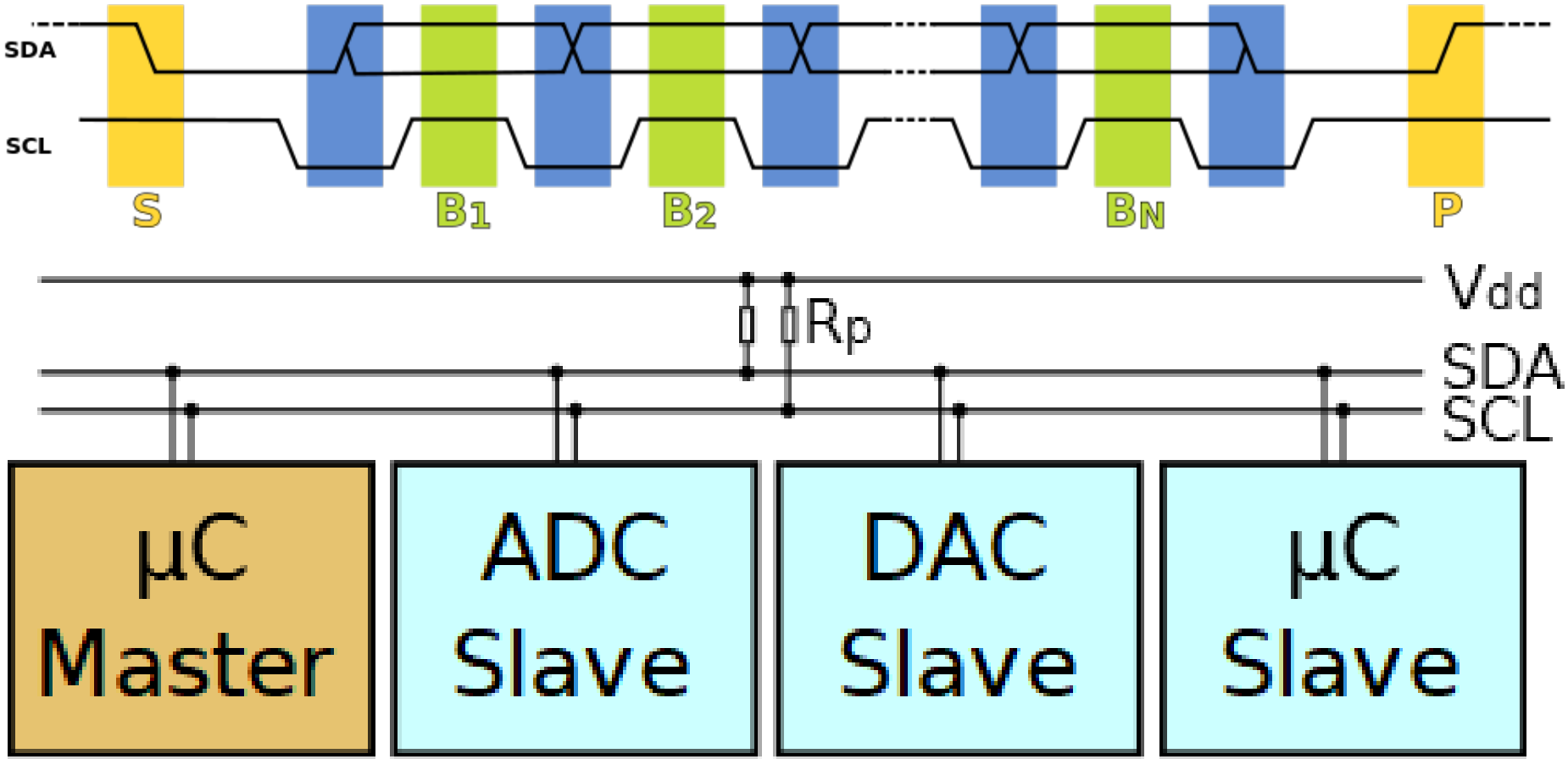
I^2C

Inter Integrated Circuit

- On PCB or between PCB
- SMBus is a subset
  - Fans, batteries, temperature, lib switches
- multiple master, multiple slave
- bitwise arbitration

Max nodes	127 or 1023
Max bitrate	3400 kbit/s
Max length	7.6 m

- developed for connecting devices on a pcb
- 2 wire bus, clock and data
- bitwise arbitration using a mechanism similar to CAN
- 7 bit field for addressing devices



UM10204 I2C-bus specification and user manual

Rev. 5, 9 October 2012

http://www.nxp.com/documents/user_manual/UM10204.pdf

http://www.i2c-bus.org/

I2C – From Wikipedia

http://en.wikipedia.org/wiki/I2C

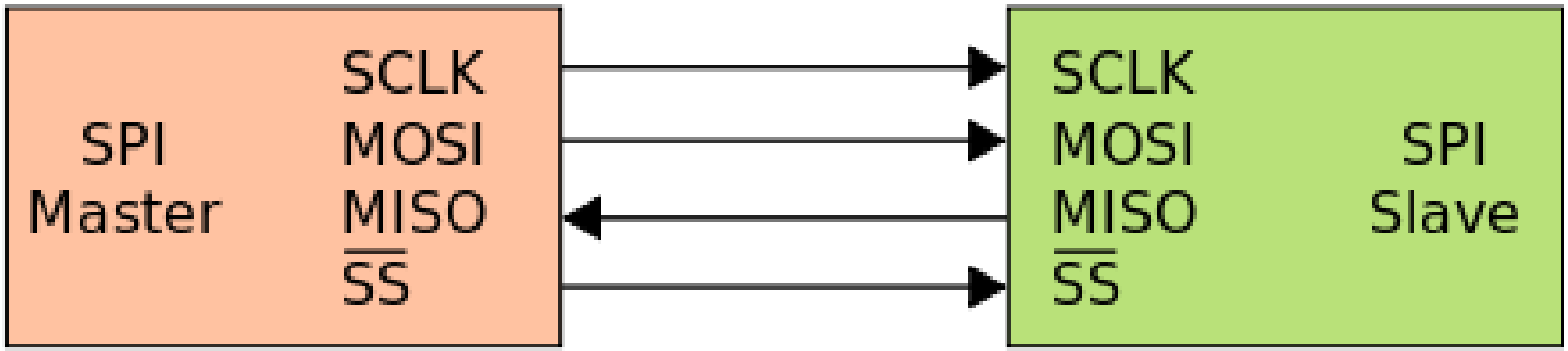
Part III

SPI
Serial Peripheral Interface

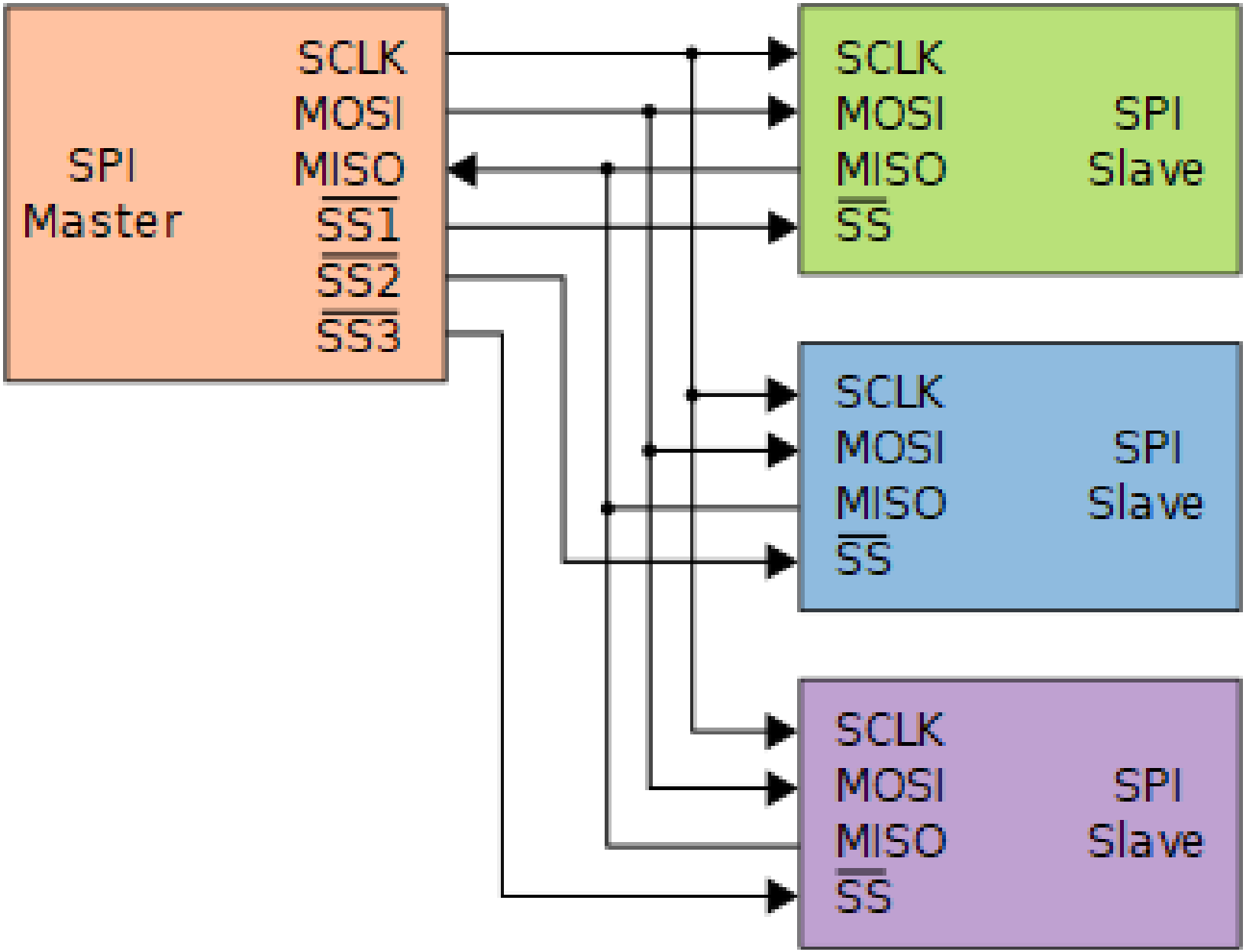
SPI

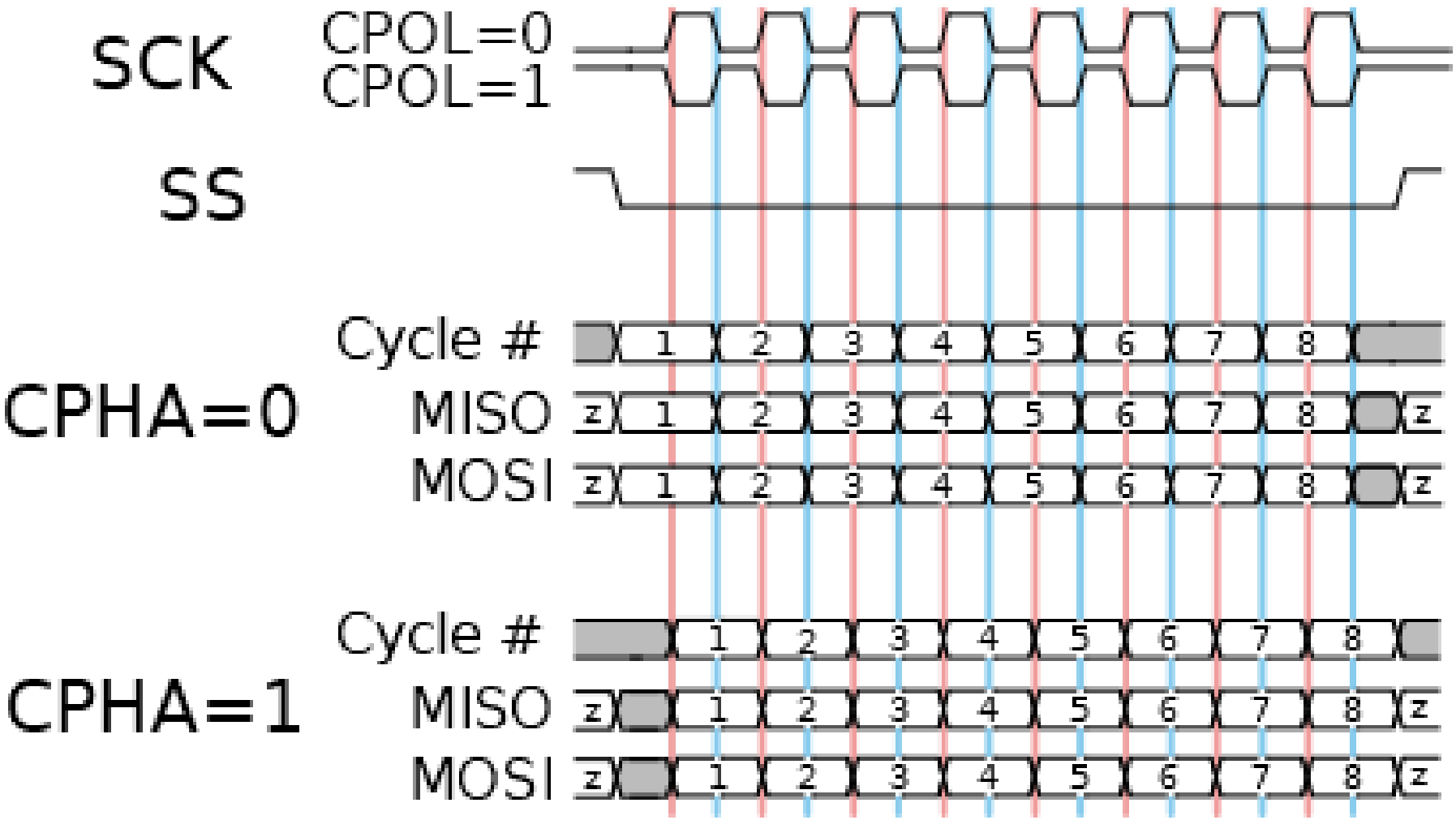
Serial Peripheral Interface

- Single master, multiple slave
- Full Duplex
  - simultaneous two way communications
- high speed data
- less PCB than parallel bus
- uses
  - MMC and SD cards
  - JTAG



- no adressing
- devices can be daisy chained
  - multiple devices share SCLK, MOSI and MISO
- device selected using dedicates SS line
- devices can respond to value set (command)


SPI
Master
SCLK
MOSI
MISO
SS1
SS2
SS3
SCLK
MOSI
MISO
SS
SPI
Slave
SCLK
MOSI
MISO
SS
SPI
Slave
SCLK
MOSI
MISO
SS
SPI
Slave


SCK
CPOL=0
CPOL=1
SS
CPHA=0
Cycle #
1 2 3 4 5 6 7 8
MISO
z 1 2 3 4 5 6 7 8 z
MOSI
z 1 2 3 4 5 6 7 8 z
CPHA=1
Cycle #
1 2 3 4 5 6 7 8
MISO
z 1 2 3 4 5 6 7 8 z
MOSI
z 1 2 3 4 5 6 7 8 z

Overview and Use of the PICmicro Serial Peripheral Interface

`http://ww1.microchip.com/downloads/en/DeviceDoc/spi.pdf`

SPI – From Wikipedia

`http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus`